WHAT IS CLAIMED IS:

1. A data processor comprising:
a random access memory;
a processing unit carrying out data processing while accessing said random access memory; and
5    a conversion unit converting data so that the number of bits having a predetermined value out of said data is at least a predetermined number for output to said random access memory when said processing unit writes said data into said random access memory.

2. The data processor according to claim 1, wherein said conversion unit includes
a detection circuit detecting, when said processing unit writes data into said random access memory, whether the number of bits having a first
5    value out of said data is at least the number of bits having a second value differing from said first value to set a flag,
a first inversion circuit inverting said data for output, and
a first select circuit responsive to the flag set by said detection circuit to selectively provide said data and said inverted data output from said first
10    inversion circuit to said random access memory.

3. The data processor according to claim 2, further comprising:
a second inversion circuit inverting data output from said random access memory for output; and
a second select circuit responsive to said flag to selectively provide
5    data output from said random access memory and said inverted data output from said second inversion circuit to said processing unit when said processing unit reads out data from said random access memory.

4. A data processor comprising:
a random access memory;
a processing unit carrying out data processing while accessing said

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random access memory;

5   a first retain circuit storing previous data output by said processing unit; and

   a subtracter taking a difference between the previous data stored in said retain circuit and current data output by said processing unit when said processing unit writes data into said random access memory.

   5. The data processor according to claim 4, further comprising a variable-length coder applying variable-length coding on difference data output from said subtracter for output to said random access memory.

   6. The data processor according to claim 4, further comprising:

   a first detection circuit detecting a data write timing of a predetermined period including the write timing of the first data out of the data write timing into said random access memory by said processing unit;

5 and

   a first selector selecting data output from said processing unit at the timing detected by said first detection circuit for output, and selecting difference data output from said subtracter at a timing other than the timing detected by said first detection circuit for output.

   7. The data processor according to claim 4, further comprising:

   a second retain circuit storing previous data output to said processing unit; and

   an adder adding difference data output from said random access

5 memory and said previous data stored in said second retain circuit.

   8. The data processor according to claim 7, further comprising a variable-length decoder applying variable-length decoding on variable-length coded difference data output from said random access memory to output the decoded data to said adder.

   9. The data processor according to claim 7, further comprising:

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a second detection circuit detecting a data readout timing of a predetermined period including the readout timing of the first data among the data readout timing by said processing unit; and

5        a second selector selecting data output from said random access memory at the timing detected by said second detection circuit for output, and selecting the data output from said adder at a timing other than said timing detected by said second detection circuit for output.

10.    A data processing method of carrying out data processing while accessing a random access memory, said method comprising the steps of:
       converting write data so that the number of bits having a predetermined value out of said write data is at least a predetermined value;
5    and
       writing said converted write data to said random access memory.

11.    The data processing method according to claim 10, wherein said step of converting write data includes the steps of
       detecting whether the number of bits having a first value out of said write data is at least the number of bits having a second value differing from
5    said first value to set a flag,
       inverting said write data for output, and
       selectively providing said write data and said inverted write data to said random access memory according to said set flag.

12.    The data processing method according to claim 11, further comprising the steps of:
       inverting data read out from said random access memory for output; and
5        selectively providing the data read out from said random access memory and said inverted read out data based on said set flag.